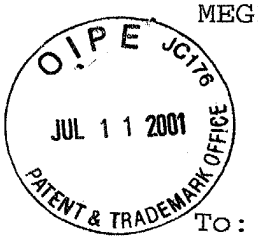
#2/ 9/13/01 2811

MEGIC-01-004



July 12, 2001

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/837,007 04/18/01

Mou-Shiung Lin, Ming-Ta Lei,
Chuen-Jye Lin

A STRUCTURE AND MANUFACTURING
METHOD OF A CHIP SCALE PACKAGE

Grp. Art Unit: 2811

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,169,329 B1 to Farmworth et al., "Semiconductor Devices Having Interconnections Using Standardized Bonding Locations and Methods of Designing", discloses a process for making a semiconductor device and the resulting device having standardized die-to-substrate bonding locations.

U.S. Patent 5,741,726 to Barber, "Semiconductor Device Assembly with Minimized Bond Finger Connections", discloses a semiconductor device assembly having external connections, including power supply connections such as to a power source or ground.

U.S. Patent 5,744,843 to Efland et al., "CMOS Power Device and Method of Construction and Layout", a CMOS power device is discussed.

U.S. Patent 5,172,471 to Huang, "Method of Providing Power to an Integrated Circuit", discloses a CMOS integrated circuit assembly for providing reduced power supply and ground inductances.

U.S. Patent 6,060,683 to Estrada, "Selective Laser Removal of Dielectric Coating", discusses a process for selectively removing a dielectric layer from a portion of a panel to create a coated and an uncoated region.

U.S. Patent 5,643,830 to Rostoker et al., "Process for Manufacturing Off-Axis Power Branches for Interior Bond Pad Arrangements", discloses a technique for improving power distribution to an semiconductur die while simultaneously reducing thermally-induced mechanical stresses on bond pads in semiconductor device assemblies.

U.S. Patent 6,160,715 to Degani et all., "Translator for Recessed Flip-Chip Package", describes a recessed chip IC package in which the IC chip is bonded to a translator, and power and ground planes for IC power and ground interconnections are formed on separate interconnect levels of the translator.

Sincerely,

George O. Saile

George O. Saile,
Reg. No. 19572